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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.

EXAMINER	
ART UNIT	PAPER NUMBER
	6

DATE MAILED:

This is a communication from the examiner in charge of this application.
COMMISSIONER OF PATENTS AND TRADEMARKS

NOTICE OF ALLOWABILITY

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance and Issue Fee Due or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

☒ This communication is responsive to the papers filed 04-10-01.

☒ The allowed claim(s) is/are 1-7.

☒ The drawings filed on 04-10-01 are acceptable as formal drawings.

☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

☒ All ☐ Some* ☐ None of the:

- ☒ Certified copies of the priority documents have been received.
- ☐ Certified copies of the priority documents have been received in Application No. _____.
- ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE FOR SUBMITTING NEW FORMAL DRAWINGS, OR A SUBSTITUTE OATH OR DECLARATION.** This three-month period for complying with the **REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL** is extendable under 37 CFR 1.136(a).

☐ Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL APPLICATION, PTO-152, which discloses that the oath or declaration is deficient. A SUBSTITUTE OATH OR DECLARATION IS REQUIRED.

☐ Applicant MUST submit NEW FORMAL DRAWINGS

- ☐ because the originally filed drawings were declared by applicant to be informal.
- ☐ including changes required by the Notice of Draftperson's Patent Drawing Review, PTO-948, attached hereto or to Paper No. _____.
- ☐ including changes required by the proposed drawing correction filed on _____, which has been approved by the examiner.
- ☐ including changes required by the attached Examiner's Amendment/Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings.

☐ Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Any reply to this notice should include, in the upper right hand corner, the APPLICATION NUMBER (SERIES CODE/SERIAL NUMBER). If applicant has received a Notice of Allowance and Issue Fee Due, the ISSUE BATCH NUMBER and DATE of the NOTICE OF ALLOWANCE should also be included.

Attachment(s)

☒ Notice of References Cited, PTO-892
☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 2
☐ Notice of Draftsperson's Patent Drawing Review, PTO-948
☐ Notice of Informal Patent Application, PTO-152
☐ Interview Summary, PTO-413
☐ Examiner's Amendment/Comment
☐ Examiner's Comment Regarding Requirement for the Deposit of Biological Material
☒ Examiner's Statement of Reasons for Allowance

SON MAI
PATENT EXAMINER

Allowable Subject Matter

1. Claims 1-7 are allowed.

2. The following is an examiner's statement of reasons for allowance: The prior art of record fails to teach a static semiconductor memory device having T-type bit line structure using horizontal memory cells to reduce layout area and increase operating speed. The static semiconductor memory device comprises: a number M x N (M: integer not less than 2; N: integer not less than 2) of memory blocks each of which include a number 8 x M of horizontal memory cells arranged in eight rows by M columns and which are arrange in M rows by N columns, a word line provided corresponding to each memory cell row of each memory block, first and second bit lines provided in common for the number M of memory block rows so as to correspond to each memory cell column, first and second bit line signal input/output lines provided corresponding to each memory block and connected to the first and second bit lines of a predetermined pair of the corresponding M pairs of the first and second bit lines, respectively, first and second data input/output lines provided corresponding to each memory block row for inputting/outputting data of the corresponding memory block row, first and second power supply lines provided corresponding to each memory block row, a global word line provided corresponding to each memory block row for selecting the corresponding memory block row, a global column selecting line provided in common for the number 11 x N of memory blocks so as to correspond to each memory cell column for selecting the corresponding memory cell column, a selection circuit responsive to an address signal for driving said word line, said global word line and said global column selecting

line to select any one memory block of said number M x N of memory blocks and any one memory cell of the number 8 x M of memory cells belonging to the memory block, a write/read circuit for writing/reading data of said memory cell, an a gate circuit for coupling a memory cell selected by said selection circuit to said write/read circuit through said first and second bit lines, said first and second bit line signal input/output lines and said first and second data input/output lines, wherein in each memory block column, the M sets of said first and second bit line signal input/output lines, said first and second data input/output lines, said first and second power supply lines, said global word lines and said global column selecting line are arranged above the number M of memory blocks respectively, and extend in the same direction as that of said word line, each set of said first and second bit line signal input/output lines, said first and second data input/output lines, said first and second power supply lines and said global word lines and said global column selecting lines are arranged above eight memory cell rows included in the corresponding memory block, respectively, said first power supply line is arranged between said first and second bit line signal input/output lines and said first and second data input/output lines, and said global word line, and said second power supply line is arranged between said first and second bit line signal input/output lines and said first and second data input/output lines, and said global column selecting line.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son Mai whose telephone number is 703-305-3497. The examiner can normally be reached on 7:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

11-15-2001

Son Mai
Examiner
Art Unit 2818